IN THE CLAIMS:

Please cancel claims 2-13 and 18-22 without prejudice or disclaimer, and add new claims 23-25 as follows:

1-22. (Cancelled)

23. (New) A computer system comprising:

one or more CPUs;

a main memory;

software means for logically dividing the computer system into a plurality of logical partitions each of which includes a subset of the main memory and a subset of CPUs that works independently from the remaining CPUs or under a time-sharing manner with the remaining CPUs; and

control means including one or more input/output adaptors, each of the adaptors being connected to an input/output device through a network, controlling outbound access of reading-out outbound data packets from said logical partitions, sending the outbound data packets to said input/output device, and controlling inbound access of writing inbound data packets, said inbound data packets being transmitted from said input/output device and stored in receive buffers provided individually for each of said logical partitions according to a destination of each inbound data packet, into said main memory,

wherein each of said input/output adaptors includes:

a send/receive allocation register for storing a value set indicating input/output performance allocation among said logical partitions as to the inbound/outbound access of said each input /output adaptor;

a send scheduler for switching a reading-out target from which the outbound data packets are read-out among said logical partitions, according to said value set stored in said send/receive allocation register;

a receive scheduler for switching a reading-out target from which the inbound data packets are read-out to write into said main memory among said receive buffers, according to said value set stored in said send/receive allocation register.

24. (New) The computer system according to claim 23, wherein said send/receive allocation register stores a number of outbound data packets to be consecutively read-out from each of the

partitions, and said send scheduler controls timings for shifting the reading-out target among the logical partitions, according to the stored number of the outbound data packets to be consecutively read-out.

25. (New) The computer system according to claim 23, wherein said send/receive allocation register stores a number of inbound packets to be consecutively read-out from each of the receiving buffers provided for each of the partitions, and said receive scheduler controls a timing for shifting the reading-out target among the receiving buffers, according to the stored number of the inbound data packets to be consecutively read-out.